1 – 5 (Deleted )

6. (Previously presented) A programmable interconnect structure to couple a first node to a second node for an integrated circuit comprising:

a power voltage and a ground voltage; and

a pull-up circuit coupled between said power voltage and said second node; and

a pull-down circuit coupled between said ground voltage and said second node; and

a programmable circuit coupled to said first node and to each of said pull-up and pull-down circuits; and

a configuration circuit including at least one memory element coupled to said programmable circuit, wherein altering the data in said at least one memory element provides a programmable method of:

decoupling said first node from second node by deactivating both said pull-up and pull-down circuits; and

coupling said first node to second node compelled by activating said pull-up and pull-down circuits.

7. (Previously presented) The structure of claim 6, wherein said first node is coupled to an output from a logic block, said logic block comprising one of fixed logic and programmable logic.

8. (Previously presented) The structure of claim 6, wherein said second node is coupled to a wire comprising a capacitive load.

9. (Original) The structure of claim 6, wherein said configuration circuit is comprised of one memory element.

10. (Previously presented) The structure of claim 6, wherein said programmable method of decoupling said first node from said second node is further comprised of isolating said second node from both pull-up and pull-down circuits.

11. (Previously presented) The structure of claim 6, wherein said programmable method of coupling said first node to said second node is further comprised of transferring a signal at said first node to said second node by the method comprised of:

deactivating said pull-down circuit and activating said pull-up circuit to provide a source current from said power voltage to said second node; and

deactivating said pull-up circuit and activating said pull-down circuit to provide a sink current ~~to~~ from said second node to said ground voltage.

12. (Previously presented) The structure of claim 11, wherein said source current and sink current strength is adjusted by sizing said pull-up and pull-down circuit transistors respectively, and wherein adjusting said source and sink current strengths provides a restored signal at said second node.

13. (Previously presented) The structure of claim 6, wherein the programmable circuit is further comprised of:

an inverter comprising an input and an output; and

a programmable method of selecting one of said first node and said ground voltage as the input of said inverter; and

the output of said inverter coupled to said pull-up circuit.

14. (Previously presented) The structure of claim 6, wherein the programmable circuit is further comprised of:

an inverter comprising an input and an output; and

a programmable method of selecting one of said first node and said power voltage as the input of said inverter; and

the output of said inverter coupled to said pull-down circuit.

15. (Previously presented) The structure of claim 6, further comprised of:

said pull-up and pull-down circuits, each comprising a pass-gate fabricated on a substrate layer; and

said configuration circuit comprising said at least one memory element fabricated substantially above said substrate layer.

16. (Previously presented) The structure of claim 15, wherein said configuration circuit is comprised one of a thin film diode, thin film resistor, thin film capacitor and a thin film transistor.

17. (Original) The structure of claim 6, wherein said memory element is comprised one of

volatile and non volatile memory element.

18. (Original) The structure of claim 6, wherein said memory element is selected from one of a fuse link, an anti-fuse capacitor, an SRAM cell, a DRAM cell, a metal optional link, an EPROM cell, an EEPROM cell, a flash cell, a ferro-electric element, an optical element and a magnetic element.

19. (Previously presented) The structure of claim 6, wherein said programmable circuit further comprises:

one or more programmable pass-gates and logic transistors located on a substrate layer; and

one or more configuration access transistors and memory transistors located on thin-film layers substantially above said substrate layer; and

one or more control signals generated from said thin film memory elements coupled to gate electrodes of said pass-gates; and

user access circuitry to change said thin film memory data via said thin film access transistors.

20. (Previously presented) The structure of claim 19, wherein the configuration circuits are located above the substrate layer by using a thin film transistor module comprising at least one of:

applying C1 mask and etching contacts;

forming W-silicide plug and performing CMP;

depositing crystalline poly-1 (P1);

performing P1 mask & etching P1;

applying blanket NMOS Vt P- implant;

applying PMOS Vt mask & N- implant;

depositing Gox;

depositing amorphous poly-2 (P2);

applying P2 mask & etching P2;

applying blanket LDN N- implant;

applying LDP mask & P- implant;

depositing a spacer oxide and etching the spacer oxide;

applying blanket N+ implantation of NMOS G/S/D;

applying P+ mask & implanting PMOS G/S/D;

depositing Nickel;

salicidizing the Nickel on the G/S/D regions & interconnect;

performing RTA anneal – P1 and P2 re-crystallization and dopant anneal;

depositing ILD oxide & CMP;

applying C2 mask & etch;

forming a W plug utilizing CMP;

depositing M1.

21. (Previously presented) The structure of claim 19, wherein the configuration circuits are located above the substrate layer by using a thin film transistor module comprising at least one of:

applying C1 mask and etching contacts;

forming W-silicide plug and performing CMP;

depositing crystalline poly-1 (P1);

performing P1 mask & etching P1;

applying blanket Gated-NFET Vt N- implant;

applying Gated-PFET Vt mask & P- implant;

depositing Gox;

depositing amorphous poly-2 (P2);

applying blanket P+ implantation of Gated-NFET Gate;

applying N+ mask & implanting Gated-PFET Gate;

applying P2 mask & etching P2;

applying blanket LDN N implant (Gated-NFET LDD);

applying LDP mask & P implant (Gated-PFET LDD);

depositing a spacer oxide and etching the spacer oxide;

depositing Nickel;

salicidizing the Nickel on exposed P1 and P2;

salicidizing P1 completely;

performing RTA anneal – P1 and P2 re-crystallization and dopant anneal;

depositing ILD oxide & CMP;

applying C2 mask & etch;

forming a W plug utilizing CMP;

depositing M1.

22. (Previously presented) A programmable interconnect structure to couple a first node to a second node for an integrated circuit comprising:

a wire having a first end and a second end; and

a first programmable interconnect structure as in claim 6, the first node of said first claim 6 structure coupled to said first node and the second node of said first claim 6 structure coupled to said first end of wire; and

a second programmable interconnect structure as in claim 6, the first node of said second claim 6 structure coupled to said second node and the second node of said second claim 6 structure, coupled to said second end of wire; and

a programmable method of coupling said first node to the wire by coupling said first claim 6 structure, and coupling said second node to the wire by coupling said second claim 6 structure; and

a programmable method of decoupling said first and second nodes from the wire by decoupling both of said first and second claim 6 structures.

23. (Currently amended) The structure of claim 22 further comprising:

~~a plurality of structures, each structure as in claim 1, each coupled between said first end of wire and an external input; and~~

a plurality of programmable wire structures to couple two nodes, each wire structure coupled between said first end of wire and an external input, each wire structure further comprised of;

a pass-gate fabricated on a substrate layer to electrically connect the two nodes; and

a configuration circuit including at least one memory element to control said pass-gate fabricated substantially above said substrate layer; and

a programmable method to select between isolating the two nodes and connecting the two

nodes by changing data stored in said memory bit; and

a programmable method of selecting at least one of said external inputs to connect to said wire.

24. (Currently amended) The structure of claim 22 further comprising:

~~a plurality of structures, each structure as in claim 1, each coupled between said second end of wire and an external input;~~ and

a plurality of programmable wire structures to couple two nodes, each wire structure coupled between said second end of wire and an external input, each wire structure further comprised of:

a pass-gate fabricated on a substrate layer to electrically connect the two nodes; and

a configuration circuit including at least one memory element to control said pass-gate fabricated substantially above said substrate layer; and

a programmable method to select between isolating the two nodes and connecting the two nodes by changing data stored in said memory bit; and

a programmable method of selecting at least one of said external inputs to connect to said wire.

25. (Currently amended) The structure of claim 22 further comprising:

~~a plurality of structures, each structure as in claim 1, each coupled between said first node and an external output; and~~

a plurality of programmable wire structures to couple two nodes, each wire structure coupled between said first node and an external output, each wire structure further comprised of:

a pass-gate fabricated on a substrate layer to electrically connect the two nodes; and

a configuration circuit including at least one memory element to control said pass-gate

fabricated substantially above said substrate layer; and

a programmable method to select between isolating the two nodes and connecting the two nodes by changing data stored in said memory bit; and

a programmable method of selecting at least one of said external outputs to connect to said first node.

26. (Currently amended) The structure of claim 22 further comprising:

~~a plurality of structures, each structure as in claim 1, each coupled between said second node and an external output; and~~

a plurality of programmable wire structures to couple two nodes, each wire structure coupled between said second node and an external output, each wire structure further comprised of:

a pass-gate fabricated on a substrate layer to electrically connect the two nodes; and

a configuration circuit including at least one memory element to control said pass-gate fabricated substantially above said substrate layer; and

a programmable method to select between isolating the two nodes and connecting the two nodes by changing data stored in said memory bit; and

a programmable method of selecting at least one of said external outputs to connect to said second node.

27. (Previously presented) A programmable interconnect structure to couple a plurality of first nodes to a plurality of second nodes for an integrated circuit comprising:

a first side comprising each of said first nodes wherein said structure originates and a second side

comprising each of said second nodes wherein said structure terminates; and

a plurality of programmable interconnect structures as stated in claim 22, each said claim 22 structure further comprising:

the first node of claim 22 structure coupled to a first node at said first side with said structure wire having the first end at said first side; and

the second node of claim 22 structure coupled to a second node at said second side with said structure wire having the second end at said second side.

28. (Currently amended) The structure in claim 27 further comprising:

~~a plurality of inputs and a plurality of interconnect structures as in claim 1, each said input connecting to the first node of said claim 1 structure, the second node of said claim 1 structure connecting to the wire first end of a said claim 22 structure at said first side; and~~

~~a plurality of outputs and a plurality of interconnect structures as in claim 1, each said output connecting to the first node of said claim 1 structure, the second node of said claim 1 structure~~ connecting to ~~a first node at said first side; and~~

a plurality of programmable wire structures to couple two nodes, each wire structure further comprised of:

a pass-gate fabricated on a substrate layer to electrically connect the two nodes; and

a configuration circuit including at least one memory element to control said pass-gate fabricated substantially above said substrate layer; and

a programmable method to select between isolating the two nodes and connecting the two nodes by changing data stored in said memory bit; and

a plurality of inputs, each said input connecting to one node of a said wire structure, the other

node of said wire structure connecting to the wire first end of a said claim 22 structure at said first side; and

a plurality of outputs, each said output connecting to one node of a said wire structure, the other node of said wire structure connecting to a first node at said first side; and

a programmable method of selecting at least one of said inputs and at least one of said outputs to connect to said first side.

29. (Currently amended) The structure in claim 27 further comprising:

~~a plurality of inputs and a plurality of interconnect structures as in claim 1, each said input connecting to the first node of said claim 1 structure, the second node of said claim 1 structure connecting to the wire second end of a said claim 22 structure at said second side; and~~

~~a plurality of outputs and a plurality of interconnect structures as in claim 1, each said output connecting to the first node of said claim 1 structure, the second node of said claim 1 structure connecting to a second~~ node at said ~~second side; and~~

a plurality of programmable wire structures to couple two nodes, each wire structure further comprised of:

a pass-gate fabricated on a substrate layer to electrically connect the two nodes; and

a configuration circuit including at least one memory element to control said pass-gate fabricated substantially above said substrate layer; and

a programmable method to select between isolating the two nodes and connecting the two nodes by changing data stored in said memory bit; and

a plurality of inputs, each said input connecting to one node of a said wire structure, the other

node of said wire structure connecting to the wire second end of a said claim 22 structure at said second side; and

a plurality of outputs, each said output connecting to one node of a said wire structure, the other node of said wire structure connecting to a second node at said second side; and

a programmable method of selecting at least one of said inputs and one of said outputs to connect to said second side.

30. (Previously presented) The structure of claim 6, further comprising a pass-gate coupled between said first and second nodes, wherein:

said configuration circuit is further coupled to said pass-gate; and

said programmable method further comprises activating said pass-gate when said programmable circuit decouples the nodes, and deactivating said pass-gate when said programmable circuit couples the nodes.

31. (Previously presented) The structure of claim 30, wherein said first node is coupled to an input/output from a logic block, said logic block comprising one of fixed logic and programmable logic.

32. (Previously presented) The structure of claim 30, wherein said second node is a wire comprising a capacitive load.

33. (Original) The structure of claim 30, wherein said configuration circuit is comprised of one memory element.

34. (Previously presented) The structure of claim 30, wherein said programmable circuit couples the nodes is further comprised of transferring a signal at said first node to said second node by the method comprised of:

deactivating said pull-down circuit and activating said pull-up circuit to provide a source current to said second node; and

deactivating said pull-up circuit and activating said pull-down circuit to provide a sink current to said second node; and

adjusting said source and sink current strengths to provide a buffered signal at said second node.

35. (Previously presented) The structure of claim 30, further comprised of:

said pass-gate fabricated on a substrate layer; and

said pull-up and pull-down circuit comprising a pass-gate fabricated on said substrate layer; and

said configuration circuit comprising the memory element fabricated substantially above said substrate layer.

36. (Original) The structure of claim 30, wherein said configuration circuit is comprised one of a thin film diode, thin film resistor, thin film capacitor and a thin film transistor.

37. (Previously presented) A programmable interconnect structure to couple a first node to a second node for an integrated circuit comprising:

a wire having a first end and a second end; and

a first programmable interconnect structure as in claim 30, the first node of said first claim 30 structure coupled to said first node and the second node of said first claim 30 structure coupled to said first end of wire; and

a second programmable interconnect structure as in claim 30, the first node of said second claim 30 structure coupled to said second node and the second node of said second claim 30 structure, coupled to said second end of wire; and

a programmable method of coupling said first node to second node by activating the first claim 30 structure pass-gate and deactivating the second claim 30 structure pass-gate, or by deactivating the first claim 30 structure pass-gate and activating the second claim 30 structure pass-gate.

38. (Previously presented) The structure of claim 30, wherein the programmable method further comprising:

providing a configuration access to alter data in stored memory element; and

generating complementary control signals from said memory element; and

controlling the polarity of said control signals by said stored memory bit polarity; and

coupling said complementary control signals to said pass-gate and pull-up and pull-down circuits; and

selecting between turning said pass-gate off and activating said pull-up and pull-down circuits, and turning said pass-gate on and deactivating said pull-up and pull-down circuits.

39. (Currently amended) The structure of claim 37, further comprising:

~~a plurality of structures, each structure as in claim 1, each coupled between said first end of wire~~

~~and an external input; and~~

a plurality of programmable wire structures to couple two nodes, each coupled between said first end of wire and an external input, each wire structure further comprised of:

a pass-gate fabricated on a substrate layer to electrically connect the two nodes; and

a configuration circuit including at least one memory element to control said pass-gate fabricated substantially above said substrate layer; and

a programmable method to select between isolating the two nodes and connecting the two nodes by changing data stored in said memory bit; and

a programmable method of selecting said external inputs to connect or disconnect to said wire.

40. (Currently amended) The structure of claim 37, further comprising:

~~a plurality of structures, each structure as in claim 1, each coupled between said second end of wire and an external input; and~~

a plurality of programmable wire structures to couple two nodes, each coupled between said second end of wire and an external input, each wire structure further comprised of:

a pass-gate fabricated on a substrate layer to electrically connect the two nodes; and

a configuration circuit including at least one memory element to control said pass-gate fabricated substantially above said substrate layer; and

a programmable method to select between isolating the two nodes and connecting the two nodes by changing data stored in said memory bit; and

a programmable method of selecting said external inputs to connect or disconnect to said wire.

41. (Currently amended) The structure of claim 37, further comprising:

~~a plurality of structures, each structure as in claim 1, each coupled between said first node and an external input/output; and~~

a plurality of programmable wire structures to couple two nodes, each coupled between said first node and an external input/output, each wire structure further comprised of:

a pass-gate fabricated on a substrate layer to electrically connect the two nodes; and

a configuration circuit including at least one memory element to control said pass-gate fabricated substantially above said substrate layer; and

a programmable method to select between isolating the two nodes and connecting the two nodes by changing data stored in said memory bit; and

a programmable method of selecting said external input/outputs to connect or disconnect to said first node.

42. (Currently amended) The structure of claim 37, further comprising:

~~a plurality of structures, each structure as in claim 1, each coupled between said second node and an external input/output; and~~

a plurality of programmable wire structures to couple two nodes, each coupled between said second node and an external input/output, each wire structure further comprised of:

a pass-gate fabricated on a substrate layer to electrically connect the two nodes; and

a configuration circuit including at least one memory element to control said pass-gate fabricated substantially above said substrate layer; and

a programmable method to select between isolating the two nodes and connecting the two nodes by changing data stored in said memory bit; and

a programmable method of selecting said external input/outputs to connect or disconnect to said

second node.

43 – 48 (Deleted)